AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A binary phase detector comprising:

a first flip flop comprising:

a data input coupled to a first signal having a first frequency, and

a clock input coupled to a second signal having a second frequency and a phase relationship with the first signal, wherein the first frequency is a multiple of the second frequency; and

a second flip flop comprising:

a data input coupled to an output of the first flip flop, and

a clock input coupled to the second signal at substantially the phase relationship with the first signal.

2. (Original) The phase detector of claim 1 wherein the first flip flop comprises a high speed flip flop.

3. (Previously Presented) A phase detector comprising:

a high speed flip flop comprising:

a data input coupled to a first signal having a first frequency, and

a clock input coupled to a second signal having a second frequency, wherein the first frequency is a multiple of the second frequency; and

a second flip flop comprising:

a data input coupled to an output of the high speed flip flop, and

a clock input coupled to the second signal;

wherein the high speed flip flop comprises at least one inductive load.

4. (Original) The phase detector of claim 2 wherein the second flip flop comprises a low speed flip flop.

5. (Original) The phase detector of claim 1 wherein the first flip flop comprises a high speed latch and a low speed latch.

6. (Original) The phase detector of claim 5 wherein the high speed latch comprises at least one inductive load.

7. (Previously Presented) A phase detector comprising:

a first flip flop comprising:

a data input coupled to a first signal having a first frequency, and

a clock input coupled to a second signal having a second frequency, wherein the first frequency is a multiple of the second frequency; and

a second flip flop comprising:

a data input coupled to an output of the first flip flop, and

a clock input coupled to the second signal;

wherein:

the data input of the first flip flop comprises a first differential input;

the data input of the second flip flop comprises a second differential input; and

the clock inputs of the first and second flip flops comprise differential clock inputs.

8. (Previously Presented) A binary phase detector comprising:

a high speed flip flop having a data input coupled to a first clock signal at a first clock frequency and a clock input coupled to a second clock signal at a second clock frequency wherein the first clock frequency is a multiple of the second clock frequency and wherein the high speed flip flop comprises a high speed latch and a low speed latch.

9. (Previously Presented) A phase detector comprising:

a high speed flip flop having a data input coupled to a first clock signal at the first clock frequency and a clock input coupled to a second clock signal at a second clock frequency

wherein the first clock frequency is a multiple of the second clock frequency and wherein the high speed flip flop comprises a high speed latch and a low speed latch;

wherein the high speed flip flop comprises at least one inductive load.

10. (Currently Amended) A method of detecting relative phase of plurality of signals, the method comprising:

providing a first signal, having a first frequency, to a data input of a first flip flop;

clocking the first flip flop using a second ~~signal,~~ signal having a second frequency and a phase relationship with the first signal, wherein the first frequency is a multiple of the second frequency;

providing an output of the first flip flop to a second flip flop;

clocking the second flip flop using the second signal at substantially the phase relationship with the first signal; and

generating at least one output signal of the second flip flop indicative of a phase difference between the first signal and the second signal.

11. (Previously Presented) The method of claim 10 wherein the at least one output signal is indicative of whether the second signal leads the first signal or whether the second signal lags the first signal.

12. (Original) The method of claim 10 comprising delaying the second signal according to the at least one output signal.

13. (Original) The method of claim 10 wherein:

the first signal comprises a first differential signal;

the output signal comprises a differential output signal.

14. (Original) The method of claim 10 comprising driving an inductive load for the first flip flop.

15. (Currently Amended) A delay lock loop comprising:

a binary phase detector comprising:

a first flip flop comprising a data input coupled to a first signal having a first frequency, a clock input coupled to a second signal having a second frequency and a phase relationship with the first signal, wherein the first frequency is a multiple of the second frequency, and at least one output; and

a second flip flop comprising a data input coupled to the at least one output of the first flip flop, a clock input coupled to the second signal at substantially the phase relationship with the first signal, and at least one output for generating at least one phase error signal;

a digital filter, coupled to receive the at least one phase error signal, that generates at least one filtered signal; and

a phase rotator, coupled to receive the at least one filtered signal and the second signal, that delays the second signal according to that at least one filtered signal.

16. (Original) The delay lock loop of claim 15 wherein the first flip flop comprises a high speed latch and a low speed latch.

17. (Currently Amended) A delay lock loop comprising:

a phase detector comprising:

a first flip flop comprising a data input coupled to a first signal having a first frequency, a clock input coupled to a second signal having a second frequency, wherein the first frequency is a multiple of the second frequency, and at least one output; and

a second flip flop comprising a data input coupled to the at least one output of the first flip flop, a clock input coupled to the second signal, and at least one output for generating at least one phase error signal;

a digital filter, coupled to receive the at least one phase error signal, that generates at least one filtered signal; and

a phase rotator, coupled to receive the at least one filtered signal and the second signal, that delays the second signal according to the at least one filtered signal;

wherein:

the first flip flop comprises a high speed latch and a low speed latch; and

the high speed latch comprises at least one inductive load.

18. (Currently Amended) A delay lock loop comprising:

a phase detector comprising:

a first flip flop comprising a data input coupled to a first signal having a first frequency, a clock input coupled to a second signal having a second frequency, wherein the first frequency is a multiple of the second frequency, and at least one output; and

a second flip flop comprising a data input coupled to the at least one output of the first flip flop, a clock input coupled to the second signal, and at least one output for generating at least one phase error signal;

a digital filter, coupled to receive the at least one phase error signal, that generates at least one filtered signal; and

a phase rotator, coupled to receive the at least one filtered signal and the second signal, that delays the second signal according to the at least one filtered signal;

wherein:

the data input of the first flip flop comprises a first differential input;

the data input of the second flip flop comprises a second differential input; and

the clock inputs of the first and second flip flops comprise differential clock inputs.

19. (Currently amended) A phase lock loop comprising:

a binary phase detector comprising:

a first flip flop comprising a data input coupled to a first signal having a first frequency, a clock input coupled to a second signal having a second frequency and a phase relationship with the first signal, wherein the first frequency is a multiple of the second frequency, and at least one output; and

a second flip flop comprising a data input coupled to the at least one output of the first flip flop, a clock input coupled to the second signal at substantially the phase

relationship with the first signal, and at least one output for generating at least one phase error signal;

a charge pump, coupled to receive the at least one phase error signal, that generates at least one current signal;

a loop filter, coupled to receive the at least one current signal, that generates at least one filtered signal; and

a delay circuit, coupled to receive the at least one filtered signal and the second signal, that delays the second signal according to the at least one filtered signal.

20. (Original) The phase lock loop of claim 19 wherein the delay circuit comprises at least one delay line.

21. (Original) The phase lock loop of claim 19 wherein the first flip flop comprises a high speed latch and a low speed latch.

22. (Currently Amended) A phase lock loop comprising:

a phase detector comprising:

a first flip flop comprising a data input coupled to a first signal having a first frequency, a clock input coupled to a second signal having a second frequency, wherein the first frequency is a multiple of the second frequency, and at least one output; and

a second flip flop comprising a data input coupled to the at least one output of the first flip flop, a clock input coupled to the second signal, and at least one output for generating at least one phase error signal;

a charge pump, coupled to receive the at least one phase error signal, that generates at least one current signal;

a loop filter, coupled to receive the at least one current signal, that generates at least one filtered signal; and

a delay circuit, coupled to receive the at least one filtered signal and the second signal, that delays the second signal according to the at least one filtered signal;

wherein:

the first flip flop comprises a high speed latch and a low speed latch; and

the high speed latch comprises at least one inductive load.

23. (Currently Amended) A phase lock loop comprising:

a phase detector comprising:

a first flip flop comprising a data input coupled to a first signal having a first frequency, a clock input coupled to a second signal having a second frequency, wherein the first frequency is a multiple of the second frequency, and at least one output; and

a second flip flop comprising a data input coupled to the at least one output of the first flip flop, a clock input coupled to the second signal, and at least one output for generating at least one phase error signal;

a charge pump, coupled to receive the at least one phase error signal, that generates at least one current signal;

a loop filter, coupled to receive the at least one current signal, that generates at least one filtered signal; and

a delay circuit, coupled to receive the at least one filtered signal and the second signal, that delays the second signal according to the at least one filtered signal;

wherein:

the data input of the first flip flop comprises a first differential input;

the data input of the second flip flop comprises a second differential input; and

the clock inputs of the first and second flip flops comprise differential clock inputs.

24. (Previously Presented) The phase detector of claim 1 wherein each data input provides a lower capacitive load than each clock input so that a lower capacitive load is provided to higher frequency signals than is provided to lower frequency signals.

25. (Previously Presented) The phase detector of claim 1 wherein the first signal comprises a first clock signal and the second signal comprise a second clock signal.

26. (Previously Presented) The phase detector of claim 1 wherein an output of the second flip flop provides a binary indication of whether the first signal leads or lags the second signal.

27. (Previously Presented) The phase detector of claim 4 wherein a signal at the data input of the low speed flip flop is of a lower frequency that the first frequency such that the low speed flip flop is adapted to operate at a lower speed than the high speed flip flop.

28. (Previously Presented) The phase detector of claim 4 wherein the data input of the low speed flip flop provides a lower capacitive load than the data input of the high speed flip flop.

29. (Previously Presented) The phase detector of claim 5 wherein a data input of the low speed latch provides a lower capacitive load than a data input of the high speed latch.

30. (Previously Presented) The phase detector of claim 8 wherein the data input provides a lower capacitive load than the clock input so that a lower capacitive load is provided to the higher frequency first clock signal than is provided to the lower frequency second clock signal.

31. (Previously Presented) The phase detector of claim 8 wherein a data input of the low speed latch provides a lower capacitive load than a data input of the high speed latch.

32. (Previously Presented) The method of claim 10 wherein each data input of each flip flop provides a lower capacitive load than each clock input of each flip flop so that a lower capacitive load is provided to higher frequency signals than is provided to the lower frequency signals.

33. (Previously Presented) The method of claim 10 wherein the first signal comprises a first clock signal and the second signal comprises a second clock signal.

34. (Currently Amended) The method of claim 10 wherein:

the first flip flop is a high speed flip ~~flop.~~ flop;

the second flip flop is a low speed flip flop; and

the output of the high speed flip flop is of a lower frequency than the first frequency such that the low speed flip flop is adapted to operate at a lower speed than the high speed flip flop.

35. (Previously Presented) The method of claim 34 wherein a data input of the low speed flip flop provides a lower capacitive load than the data input of the high speed flip flop.

36. (Previously Presented) The method of claim 34 wherein:

the high speed flip flop comprises a high speed latch and a low speed latch; and

a data input of the low speed latch provides a lower capacitive load than a data input of the high speed latch.

37. (Previously Presented) The method of claim 10 wherein the first and second signals are provided to a binary phase detector that performs the providing, clocking and generating.